WHAT IS CLAIMED IS:

1. An apparatus including a multistage differential amplifier with commonly controlled input and output common mode voltages, comprising:

first and second differential input terminals to convey first and second phases of a differential input signal with an associated input common mode voltage;

first and second differential output terminals to convey first and second phases of a differential output signal corresponding to said differential input signal with an associated output common mode voltage;

a common mode control terminal to convey a common mode control signal for jointly controlling said input and output common mode voltages; and

a plurality of differential amplifier circuits successively coupled between said common mode control terminal, said first and second differential input terminals, and said first and second differential output terminals, wherein

each one of said plurality of differential amplifier circuits includes first and second amplifier input terminals, first and second amplifier output terminals, an input control terminal and an output control terminal,

a first one of said plurality of differential amplifier circuits is coupled to said first and second differential input terminals via said first and second amplifier input terminals, and is further coupled to said common mode control terminal via said input control terminal,

a last one of said plurality of differential amplifier circuits is coupled to said first and second differential output terminals via said first and second amplifier output terminals, and

said first and second amplifier input terminals and said input control terminal of each succeeding one of said plurality of differential amplifier circuits is coupled to said first and second amplifier output terminals and said output control terminal, respectively, of a preceding one of said plurality of differential amplifier circuits.

2. The apparatus of claim 1, wherein each one of said plurality of differential amplifier circuits comprises:

a first circuit branch including said first amplifier input and output terminals;

a second circuit branch including said second amplifier input and output terminals; and

a third circuit branch including said input and output control terminals.

3. The apparatus of claim 2, wherein each one of said plurality of differential amplifier circuits further comprises a shared terminal via which said first, second and third circuit branches are mutually coupled.

4. The apparatus of claim 2, wherein each one said first, second and third circuit branches of at least said first one of said plurality of differential amplifier circuits comprises a plurality of telescopically coupled NMOS transistors.

5. The apparatus of claim 2, wherein each one said first, second and third circuit branches of at least said last one of said plurality of differential amplifier circuits comprises a plurality of telescopically coupled CMOS transistors.

6. The apparatus of claim 1, further comprising:

a first biasing circuit coupled to a portion of said plurality of differential amplifier circuits and responsive to a first bias current by providing at least a first bias voltage thereto; and

a second biasing circuit coupled to another portion of said plurality of differential amplifier circuits and responsive to a second bias current by providing at least a second bias voltage thereto.

7. The apparatus of claim 6, wherein said first biasing circuit is further coupled to said common mode control terminal and responsive to said first bias current and said common mode control signal by providing said at least a first bias voltage.

8. An apparatus including a multistage differential amplifier with commonly controlled input and output common mode voltages, comprising:

input differential amplifier circuitry including

first and second input amplifier input terminals for reception of first and second phases of a differential input signal with an associated input common mode voltage,

first and second input amplifier output terminals,

an input amplifier control input terminal for reception of a common mode control signal, and

an input amplifier control output terminal;

intermediate differential amplifier circuitry including

first and second intermediate amplifier input terminals coupled to said first and second input amplifier output terminals,

first and second intermediate amplifier output terminals,

an intermediate amplifier control input terminal coupled to said input amplifier control output terminal, and

an intermediate amplifier control output terminal; and

output differential amplifier circuitry including

first and second output amplifier input terminals coupled to said first and second intermediate amplifier output terminals,

first and second output amplifier output terminals for conveyance of first and second phases of a differential output signal corresponding to said differential input signal with an associated output common mode voltage corresponding to said input common mode voltage,

an output amplifier control input terminal coupled to said intermediate amplifier control output terminal, and

an output amplifier control output terminal.

9. The apparatus of claim 1, wherein said input differential amplifier circuitry, said intermediate differential amplifier circuitry and said output differential amplifier circuitry each comprises:

first branch circuitry including said first amplifier input and output terminals;

second branch circuitry including said second amplifier input and output terminals; and

third branch circuitry including said input and output control terminals.

10. The apparatus of claim 9, wherein said input differential amplifier circuitry, said intermediate differential amplifier circuitry and said output differential amplifier circuitry each further comprises a shared terminal via which said first branch circuitry, said second branch circuitry and said third branch circuitry are mutually coupled.

11. The apparatus of claim 9, wherein said first branch circuitry, said second branch circuitry and said third branch circuitry of said input differential amplifier circuitry comprises a plurality of telescopically coupled NMOS transistors.

12. The apparatus of claim 11, wherein said first branch circuitry, said second branch circuitry and said third branch circuitry of said intermediate differential amplifier circuitry comprises another plurality of telescopically coupled NMOS transistors.

13. The apparatus of claim 9, wherein said first branch circuitry, said second branch circuitry and said third branch circuitry of said output differential amplifier circuitry comprises a plurality of telescopically coupled CMOS transistors.

14. The apparatus of claim 8, further comprising:

first biasing circuitry coupled to at least said input differential amplifier circuitry and responsive to a first bias current by providing at least a first bias voltage thereto; and

second biasing circuitry coupled to said output differential amplifier circuitry and responsive to a second bias current by providing at least a second bias voltage thereto.

15. The apparatus of claim 14, wherein said first biasing circuitry is further coupled to said input amplifier control input terminal and responsive to said first bias current and said common mode control signal by providing said at least a first bias voltage.

16. An apparatus including a multistage differential amplifier with commonly controlled input and output common mode voltages, comprising:

input amplifier means for receiving a common mode control signal and an input differential signal with an associated input common mode voltage and in response thereto providing a first intermediate differential signal and a first intermediate control signal, wherein said input common mode voltage is controlled by said common mode control signal;

intermediate amplifier means for receiving said first intermediate differential signal and said first intermediate control signal and in response thereto providing a second intermediate differential signal and a second intermediate control signal; and

output amplifier means for receiving said second intermediate differential signal and said second intermediate control signal and in response thereto providing an output differential signal corresponding to said input differential signal with an associated output common mode voltage corresponding to said input common mode voltage.

17. The apparatus of claim 16, further comprising:

first biasing means for receiving a first bias current and in response thereto providing at least a first bias voltage for at least said input amplifier means; and

second biasing means for receiving a second bias current and in response thereto providing at least a second bias voltage for said output amplifier means.

18. The apparatus of claim 17, wherein said first biasing means is for receiving said first bias current and said common mode control signal and in response thereto providing said at least a first bias voltage.